ABSTRACT

An apparatus for the on-chip testing random access memory arrays. In representative embodiments, circuitry is disclosed which provides the ability to test random access memory arrays on-chip by means that do not required substantial area on the chip. The circuits disclosed are inherently located closer to the tested area which reduces propagation delay errors. These advantages have been obtained by locating the circuitry necessary to perform such test in the addressing and input/output blocks of the RAM.